EE 4250 **Digital Integrated Circuits** **Spring 2008**

Catalog Description	Prereq.: EE 3220, 3221, and 3232. 2 hrs. lecture; 2 hrs. lab. ABET category: 2 hrs. design; 1 hr. engineering science. Analysis and design of digital integrated circuit logic gates in bipolar and MOS technology; semiconductor memories and their operations.
Instructor	Dr. Dooyoung Hah, 229 EE Building. Ph: 578-5532. dyhah@lsu.edu
Lecture	MW 8:40 – 9:30 AM, 3131 Patrick Taylor Hall
Laboratory	T 3:40 – 5:30 PM, 252 EE Building
Office Hours	MW 9:40 – 11:10 AM, T 9:00 – 11:00, other times by appointment only
Course Homepage	http://www.ece.lsu.edu/dyhah/ee4250_spring2008/ee4250_spring2008.html
Textbook	D. A. Hodges, H. G. Jackson and R. A. Saleh, Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology, McGraw-Hill, 3rd Edition, 2003.
Topics Covered	✓ Introduction ✓ Bipolar transistor logics ✓ MOS transistor ✓ MOS inverter circuits ✓ Static MOS gate circuits ✓ High-speed CMOS logic design ✓ Transfer gate and dynamic logic design ✓ Semiconductor memory design * Note: Not all topics may be covered, and some related material not listed above may be included.

Grading Policy	The points are accumulated in the following manner: ✓ Homework 10% ✓ Attendance 5% ✓ Laboratory 25% ✓ Test 1 (in-lecture) 20% (Feb. 25, M) ✓ Test 2 (in-lecture) 20% (Apr. 2, W) ✓ Final exam 20% (May 5, M 5:30-7:30PM) Total: 100% • Each unexcused absence will deduct 0.2% point. • Final letter grades will be given based on the following criterion. - Graduate students ***A***: > 85, ***B***: 84.9─65, ***C***: 64.9─50, ***D***: 49.9─40, ***F***: < 39.9 - Undergraduate students ***A***: > 85, ***B***: 84.9─75, ***C***: 74.9─65, ***D***: 64.9─55, ***F***: < 54.9

Regrade Policy:

All questions regarding the grading of any assignment/exam except the final exam are handled *exclusively* through *written* request and will *only* be accepted within the first week after grading is completed, announced in class and the assignment is made available. To submit a regrade request, print/type your name on a separate sheet of paper and include a concise explanation of all your concerns/questions and JUSTIFY why you think you deserve additional credit. *Staple* this sheet to the front of your graded assignment/exam and resubmit it to your instructor during office hours. The assignment will be regraded in its entirety and returned to you. If you continue to have concerns, arrange for an appointment with your instructor to discuss the issue.

Examinations / Quizzes / Homeworks / Absence:

Examinations are given on the dates indicated above. Schedule conflicts must be resolved prior to the exam date and **NO** makeup exams are given. All exams will be closed book, closed notes. Calculators may or may not be allowed depending on the examination content (i.e. learn to think without them!). When allowed, calculators may only be used for simple algebraic and trigonometric operations (i.e. no programmable features).

Quizzes may be given throughout the semester either in the beginning or at the end of lecture but will not be graded.

Late homework submission will not be accepted and no credits will be given.

Class attendance is the responsibility of the student. The student is expected to attend all classes. A student who finds it necessary to miss class assumes responsibility for making up examinations, obtaining lecture notes, and otherwise compensating for what may have been missed. The course instructor will determine the validity of a student's reason(s) for absences and will assist those students who have valid reasons. Valid reasons for absences include:

1. Illness
2. Serious family emergency
3. Special curricular requirements such as judging trips or field trips
4. Court-imposed legal obligations such as subpoenas or jury duty
5. Military obligations
6. Serious weather conditions
7. Religious observances.
8. Participation in varsity athletic competitions or university musical events

The student is responsible for providing reasonable advance notification and appropriate documentation of the reason for the absence.

General Class Procedures and Office Hours:

Students are responsible for all announcements made in lecture. Course information, announcements and grades will also typically be posted on the course website or on your instructors' door. It is a sound practice to check these locations periodically for important updates and information you may have missed.

Assistance is available from the instructor during office hours; however, do not expect him to do your homework for you! Carefully prepare your questions beforehand and answer as many of them as possible for yourself. Please observe the posted office hours for this course and confine your visits to those time slots. If the posted hours conflict with your schedule, you can make an appointment and alternate arrangements will be made to accommodate you. DON'T WAIT UNTIL THE LAST MINUTE TO ASK FOR HELP!

LEARN TO USE ELECTRONIC MAIL (E-MAIL)! You are encouraged to use your PAWS computer account and electronic mail as this is a great way to communicate with your instructor for this course. It will improve the response time for most of your questions and effectively extends office hours during which you can get questions answered. Your instructor regularly checks and responds to his email. Students NOT using the PAWS account should have it set to forward all campus correspondence.

EE 4250 Laboratory **Digital Integrated Circuits** **Spring 2008**

Instructor: Dr. Dooyoung Hah (dyhah@lsu.edu) – Section 3, T 3:40 – 5:30 pm

Lab Instruction: Handouts (will be distributed at the first lab session and is posted at the course website as well.)

Lab Schedule:

- ✓ Lab#0 (1/22): Laboratory instrumentation
- ✓ Lab#1 (1/29): Bipolar transistor inverter
- ✓ Lab#2 (2/12): Voltage transfer characteristics of TTL gates
- ✓ Lab#3 (2/19): TTL and CMOS gates delay
- ✓ Lab#4 (2/26): Voltage transfer characteristics of MOS inverters
- ✓ Lab#5 (3/4): Noise in a CMOS inverter chain
- ✓ Lab#6 (3/11): CMOS NAND and NOR gate characteristics
- ✓ Lab#7 (3/25): CMOS SR latch and JK flip-flop
- ✓ Lab#8 (4/1): D flip-flops and latches
- ✓ Design project (4/8): Static MOS gate circuits
- ✓ Lab#9 (4/15): MOS pass gates and T-gate
- ✓ Lab#10 (4/22): Dynamic logic gate circuits
- ✓ Makeup lab (4/29)

* The schedule above may be changed if necessary.

General Grading Policy:

- ✓ Perfect score for each lab session is 10 points.
- ✓ Unreasonable discussion or illogical data interpretation → " – 1"
- ✓ Lack of discussion or data interpretation → " – 2"
- ✓ Unreasonable experiment results → " – 1" to " – 2"
- ✓ Unreasonable SPICE simulation results → " – 1"
- ✓ Lack of SPICE simulation results → " – 2"
- ✓ Late reports → " – 1" per week
- ✓ "0" is the minimum score.
- ✓ Missing lab: zero point.

Notes: 1. You should be ready for each lab. That includes,

- To read and understand the lab instruction before each lab session
- **To perform SPICE simulation and bring the results**
- To complete the report for the previous lab before the new lab session starts

- To show up on time

2. For each lab except the Lab #0, a report must be submitted to the instructor on the following lab session before the session starts. Every student (**not every group!**) must compose a report. Each report can be organized as following:
    a. Objective
    b. Circuit diagram
    c. Experimental observations
    d. Interpretation of the data, discussion, difficulties, etc.
    e. (Optional) Revised PSPICE simulation results

    Other tips:
    - It is discouraged to simply copy the theory to the reports. Additional theoretical backgrounds or discussion, on the other hand, is welcomed.
    - Some lab sessions require SPICE simulation beforehand. If a session demands as such, the results must be brought in for the session and submitted right after the session is finished.
    - Write the name of your lab partner on the cover page.

3. Laboratory etiquettes
    - Take a good care of the lab instruments. If you are not sure what you are doing, it is better to ask than to *go for it*.
    - Do not eat or drink in the lab.
    - Clean your table as much as you can before you leave the lab. That includes returning the components to their original locations and turning off the instruments.

4. Useful tips
    - Circuit connection: try to be neat and shorten the wiring. Messy wiring is not only easy to cause an error but also hard to debug. Use a color of wire as an indication. For example, red wires for positive voltage supply, blue wires for negative voltage supply, black wires for ground, green wires for signal, etc.
    - It has been brought to the instructor's attention that some parts of some breadboards have defects. Also some active devices such as transistors, diodes, logic gates, etc, might not be working. If you suspect such things, move your circuit to other part of the breadboard or replace the suspicious components.
    - If you feel that there has been no progress for long time, ask the instructor for

help. Don’t wait until the last minute.

- If you have an *inevitable* need to miss a lab session, contact the instructor as early as possible so that proper arrangement can be made. For example, medical emergency, family emergency, and job interview, are reasonable excuses.